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B. Tech 7th Semester Examination

CMOS & VLSI Design (NS)

EC-415

Time : 3 Hours **Max. Marks : 100**

The candidates shall limit their answers precisely within the answer-book (40 pages) issued to them and no supplementary/continuation sheet will be issued.

Note : Attempt any one question each from section A, B, C, and D. Section E is compulsory.

SECTION - A

1. (a) Draw labeled Y-chart for different VLSI design styles. Discuss its level to level correlation between physical structural and behavior model. (8)

   (b) Draw the voltage transfer characteristics of CMOS inverter and show the operating regions on it of PMOS and NMOS. If the supply is V_{DD}= 5.0 V_{thn}=0.6 V, V_{thp}=–0.6 V then find the operating region of PMOS and NMOS in a CMOS inverter if input is 2.5 volt. (12)

2. (a) What is device modeling? Draw the complete model of a MOSFET and modify it under body bias. (8)

   (b) How mobility difference of PMOS and NMOS is compensated to achieve a symmetrical inverter?

   (i) If the mobility of electron is 2.5 times of hole then find the ratio of PMOS and NMOS area for a symmetrical CMOS inverter.

   (ii) If the mobility of electron is 2.5 times of hole then find the ratio of T_{ON} to T_{OFF} time in a uncompensated CMOS inverter. (12)

SECTION - B

3. (a) What are the different components of a node capacitance in integrated circuit? Discuss the contribution of device and interconnect capacitance in it. Discuss the method to find the propagation delay between two node in an ICs. (10)

   (b) Draw the logic circuit of a CMOS implementation for Y = ABC + C (D + E). If the minimum feature size is 20 micron then calculate the total transistor area for this implementation when size of PMOS and NMOS have been properly adjusted. (10)

4. (a) Define clock skewing. How this problem is solved in ICs? Describe any one clock scheme used in ICs. (10)

   (b) Draw a CMOS circuit for Y = AB + CDE and design the (W/L) ratio of each transistor such that the over all (W/L) ratio of pull up stage is 60 and pull down is 20. (10)

SECTION - C

5. (a) What is Eular path? How it is used for layout optimization? Draw the complete layout for a sum out of single bit full adder. (10)

   (b) Draw the circuit of different memory cell used in static cases. Compare these with dynamic cell. (10)

6. (a) Explain the working of a sequential adder. Compare it with a parallel adder in respect of hardware and speed. Find the ratio of speed of such adder for addition of two 4-bit data. (10)

   (b) What is latch-up problem? How it is formed? How it can be avoided? Draw the circuit of a latch up formation in CMOS circuit. (10)

[P.T.O.]

SECTION - D

7. (a) Implement Boolean function Y = ABC + bar(DE) in PAL. (10)

   (b) Compare application specific IC design (ASIC) with full custom design. Why the cost of full custom is more? Explain it with an example. (10)

8. (a) Explain the working of a sequential adder. Compare it with a parallel adder in respect of hardware and speed. Find the ratio of speed obtained in a sequential adder and parallel adder for addition of two 4-bit data. (10)

   (b) Draw the circuit of any digital multiplier. Find the number total adder used in a 4 bit multiplier. Compare the different multiplier circuits. (10)

SECTION - E (Compulsory)

9 (i) If V_{OH}=3.5V, V_{OL} =0.5 V,V_{IH} =1.5 V, V_{IL} =2.5 V then calculate the noise margin for low (NML) and noise margin for high (NMH).

(ii) Draw the Voltage Transfer characteristics (VTC) of a resistive load inverter.

(iii) Find the modified power dissipation and device area when full scaling is used when dimensions are scale down by a factor of S = 0.8.

(iv) Draw the changes of Oxide capacitance C_{gs} when the device operates in linear and saturation.

(v) If the load Capacitance of a CMOS inverter is 200pf and its supply voltage is 5.0 V then calculate the power loss when it operates on 20 kHz.

(vi) Draw the construction of a depletion mode n-channel MOSFET.

(vii) Write any three Design rule check (DRC) to be followed in layout.

(viii) Draw the different symbols used for CMOS Transmission gates.

(ix) Find the number of pull up transistor used in Y = AB+CD.

(x) Write two advantages of Domino logic. (2×10=20)